Peak Detector using Low Voltage Operational Transresistance Amplifier

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Abstract- *Previously, peak detector was build using diode, capacitor and a voltage mode device i.e. Op-Amp. Due to emergence of current mode circuits, it is possible to design high gain, large bandwidth, high speed and low voltage analog signal processing and generating applications. OTRA (Operational transresistance amplifier) is in fashion to design these applications due to its various advantages. In this paper, peak detector is proposed using low voltage OTRA. This proposed circuit is simulated using PSPICE simulation for which OTRA is realized using 180 nm CMOS process with low power supply of ±0.9V. The proposed circuit also provide very low power dissipation.*

Keywords: *Peak Detector, OTRA, current mode circuits*

I. INTRODUCTION

With the rise of portable electronics and communication systems, low voltage and low power circuit design has gained some popularity. The main aim of integrated circuit design techniques is to achieve high speed and high integration on chip with a large dynamic range. One of the factors, which affect these parameters, is power dissipation in the circuit. This paper is focused on the reduction of power dissipation for high performance system. For high frequency applications, current-mode approach is preferred rather than the traditionalvoltage-mode structures.OTRA is very interesting current mode circuit to achieve high gain, wide bandwidth, greater linearity and large dynamic range. OTRA has low input and output impedances and hence negligible parasitic capacitance at input terminals.

Peak detector has various applications in measurement circuits and communication receivers like directional couplers, low power watt meters, RF millivoltmeters, radio receivers etc. Various peak detector topologies are already available in many literatures. [2-4] Earlier peak detector circuit can be designed by using simple connection of diode and capacitor.Due to non-linear characteristics of diode, this circuit does not track the input precisely and hence not suitable for detecting small signal of voltage less than 0.6 V. The voltage drop across the diode can be removed by connecting an op-amp in feedback of diode to get the more linear peak detector. But the slew rate is finite and limiting the speed of the circuit.[2,5-7] In integrated circuits, a diode-connected MOS transistor or a source follower can replace the non-linear diode. [8] In this paper, a topology of active positive peak detector given in [2] is implemented using OTRA. The OTRA is realized using 180 nm CMOS process with power supply of ±0.9V. The implemented circuit has the advantage of low power dissipation.

II. REALIZATION TOPOLOGY OF PRECISION PEAK DETECTOR

The several types of peak detector topologies are discussed in [2], one of them is shown in Fig. 1. The diode and capacitor connected peak detector does not provide better results due to non-linearity of diode. So, the diode can be replaced by diode connected transistor or a source follower. The generalized idea of positive peak detector using source follower presented in [2] is briefly reviewed here. An operational transresistance amplifier could follow the peak detector for isolation.

In Fig. 1, if the applied input voltage V_{in} exceeds the voltage across capacitor, the transistor M is on and charges the capacitor C.Similarly, if V_{in} comes below the voltage across capacitor, transistor M is off, and the capacitor holds the output peak voltage.

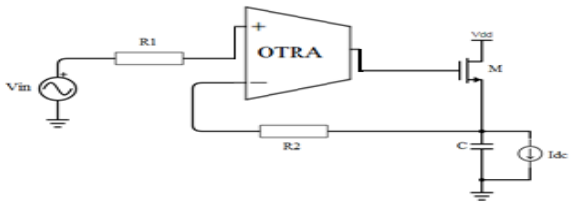

Fig. 1. Positive Peak Detector using OTRA

A small current source, I_{dc}or a resistor is connected across the capacitor C to discharge the capacitor for better tracking. The voltage across the capacitor, V_p is given as:

$$Vp = \frac{1}{C}\int idt$$

$$i = C\frac{dVp}{dt}$$

$$\frac{dVp}{dt} = \frac{i}{C}$$

This change in voltage across capacitor i.e. $\frac{dVp}{dt}$ is known as droop rate. It means droop rate completely depends on the capacitor C and small current source I_{dc}. This droop rate should be carefully determined in designing an automatic gain control loop. The droop rate can be affected by leakage current, so the parasitic capacitances should be considered. If the peak detector has low droop rate, the capacitor C discharges slowly while the envelope of an input signal keeps decreasing faster below the previous peak voltage, in this case the V_p cannot follow the V_{in} fast enough. Thus, to quickly follow the next input peak point, the peak detector needs to be reset periodically. A NMOS switch across the capacitor C is connected to reset the output instantly to zero.[2]

III. OTRA BASED PEAK DETECTOR

Operational transresistance amplifier (OTRA) is a three-terminal analog device which is characterized by the following matrix:

$$\begin{bmatrix} V_+ \\ V_- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_o \end{bmatrix}$$

Ideally, the transresistance gain R_m approaches infinity and applying external negative feedback will force the two input currents to be equal. The symbol of the OTRA is shown in Fig. 2. The input terminals are insensitive to stray capacitances and provided low input impedance. There are many topologies for CMOS realization of OTRA which are already available in literature. [10-13]

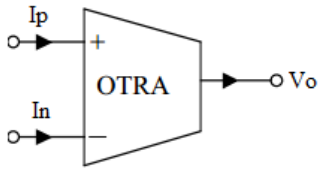

Fig. 2. Symbol of OTRA

The CMOS realization of OTRA in [12] is shown in Fig. 3 and is used as a buffer amplifier to follow the peak detector for isolation in this proposed paper.

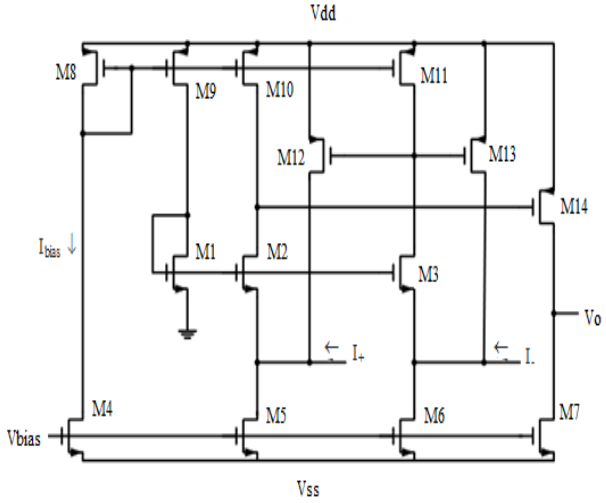

Fig. 3. CMOS Realization of OTRA [12]

In the OTRA basedpeak detector the output of OTRA is connected to the gate terminal of transistor M which decide the charging and discharging of capacitor C. The positive input terminal of OTRA is connected to the input voltage V_{in} and negative terminal is connected to the source of transistor M.

IV. SIMULATION RESULTS

The proposed peak detector is simulated using 180 nm process. The OTRA structure [12] is analyzed with supply voltage of ±0.9V. The simulated result of the OTRA is shown in Fig. 4 and tabulated in table 1.

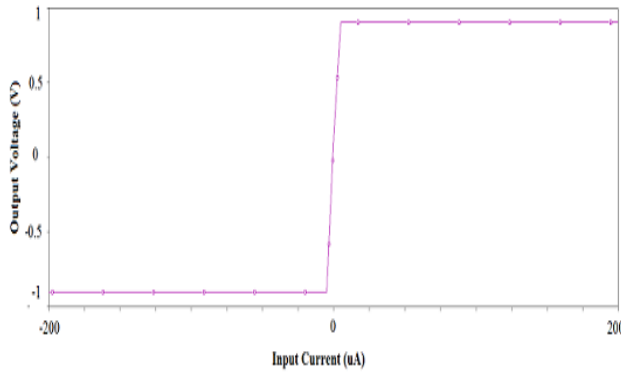

Fig. 4 (a). DC Analysis of simulated OTRA

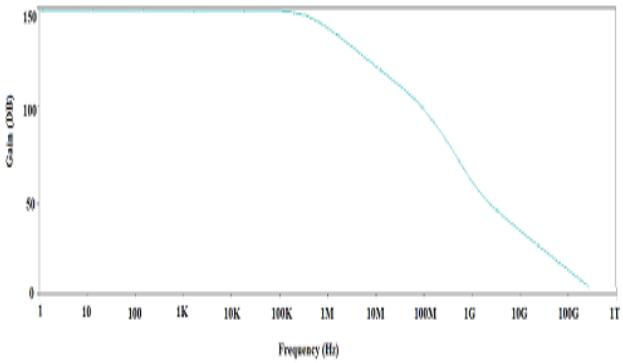

Fig. 4 (b). AC Analysis of simulated OTRA

Parameters	Values
Open loop transresistance gain	150 DB
Unity gain bandwidth	500 GHz
Cut-off frequency	500 KHz
Power Dissipation	0.086mW

Table 1.Summary Table of simulated CMOS OTRA

Fig. 5 shows the simulation results of the proposed peak detector with resistanceR1=R2=1KΩ, capacitance, C=1nF and switching current source, I_{bias}=10uA. The applied input voltage, V_{in} is 0.5 V. Fig 5(a), 5(b) and 5(c) shows the simulation results for 50 MHz, 100 MHz and 500 MHz input signal respectively.

Those input signals are amplitude-modulated with different modulation frequencies. By switching the hold capacitor and the current source simultaneously, the peak detector can efficiently track the peak over time.

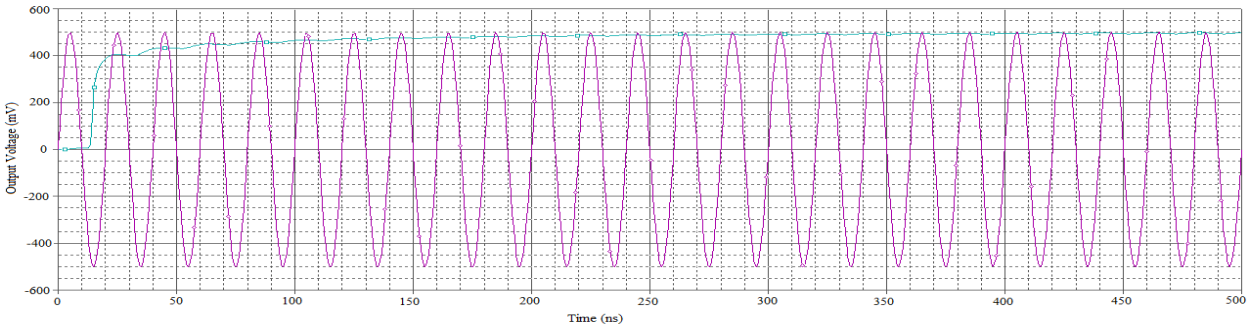

Fig. 5 (a). Output Voltage of OTRA based Peak detector for 50 MHz input signal

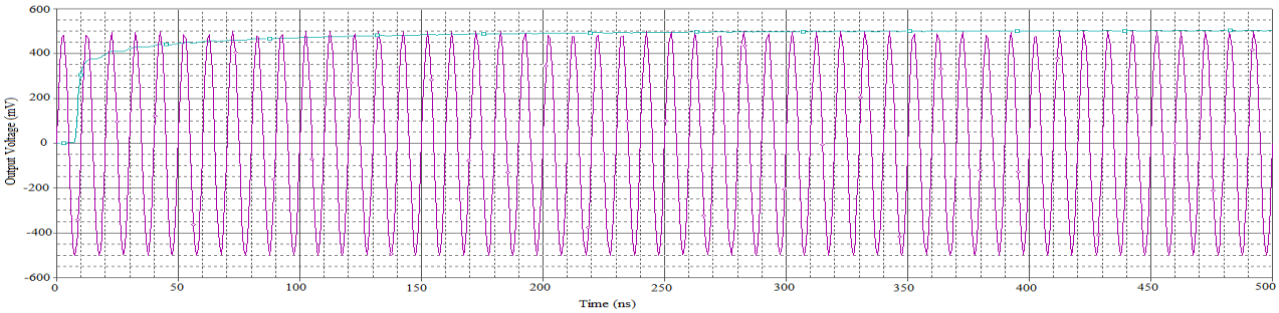

Fig. 5 (b). Output Voltage of OTRA based Peak detector for 100 MHz input signal

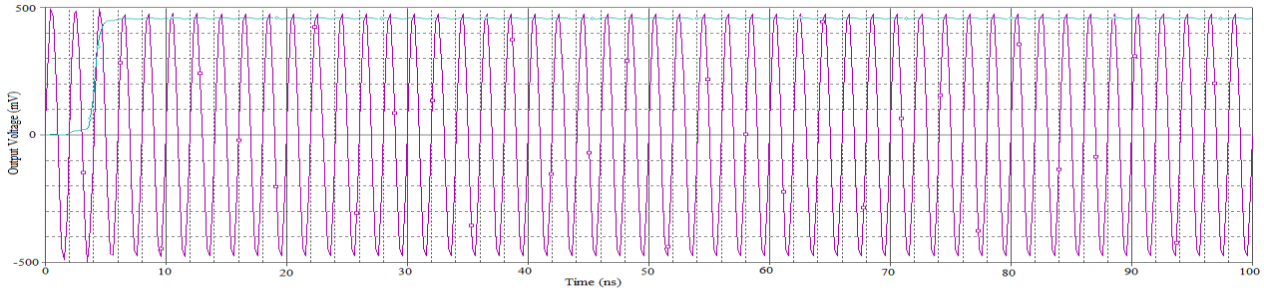

Fig. 6(c). Output Voltage of OTRA based Peak detector for 500 MHz input signal

V. CONCLUSION

A peak detector based on OTRA is presented wherein OTRA act as a buffer which could follow the peak detector for isolation. The workability of the proposed peak detector is verified through SPICE simulations. The proposedpeak detector can be used as an important building block in wireless communication receivers.

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