Development of a Local Area Electronic Policing System for Security Enhancement

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Abstract

Electronic policing system is becoming more and more appreciated than State and Community based policing, with its attendant advantages of prompt information dissemination and retrievals, ease of documentation, as well as in- the act apprehension of criminals support for ease of judgment. In this work, the design of a Local Area Electronic Policing System for a typical local policing station covering a large area or community is presented. The local Area Electronic Policing System consists of a receiver, and Local Area Electronic policing controller (LAEPC). The receiver circuit consists of an AM receiver and a comparator circuit. The basic purpose of a receiver is to receive an RF signal, amplify it, filter it to remove unwanted signals, and recover the desired base band information. The LAEPC input is the digital output signal from the receiver circuit. The LAEPC converts the serial information received to parallel information which is transferred to the microcontroller 80CH51 circuit, which works on the received signals, to generate the required code, from the developed program, to the on –line microcomputer for interpretation; being used to locate the distress point of call DPOC address and relevant information on the distress caller from the system database. The response of the receiving rf amplifier gives an output voltage of 660mV for an input response of 18mV, further amplified using common source FET amplifier to give 4.5V; with bode-plot response of the receiver to the incoming signals giving a resonant frequency of 483.35kHz and a gain of 27.734dB. The reliability of the design LAEPC was determined to give 74.5% for continuous operation in a year. The designed LAEPC with its attachments in conjunction with the use One touch Sender OTS from the distress caller end , will increase the "caught- in the –act" scheme as against the present "after –the- act " investigations being adopted by the Police to combat crime in developing Countries. The "caught- in the –act" scheme is necessary to prove the case of criminality beyond any reasonable doubt, in a law court.

Keywords - *Local policing Station, Local electronic policing controller, Receiver, Comparator, Microcontroller.*

I. INTRODUCTION

Policing an environment , cities or a nation for effective law and order maintenance is one of the fundamental constitutional requirements of a nation for equal checks and balances. The mode of policing and monitoring of citizen differ from one country to another, but , all do have a police organization, for the prevention of crimes, with its own communication system[1],[2].

In the developed world, the internet is used extensively, for prompt reporting and tracking of criminals [3]-[6]. This involves the use of internet cameras for tracking and prompt deployment of police officers to the scene , as well as other electronic gadgets made available through patrol vehicles, with huge investment in ICT to increase the capacity of storage of information and processing of large volume of data, to improve their intelligence and investigative capabilities [5]-[8].

The huge investment in ICT required for modern policing in many developing countries, is out of reach within their budgetary accommodation, and thus, many still operates with the traditional policing with heavy reliance on foot, motorcycles and patrol vehicles. It is said [2],[5],[9] that about 3 billion dollars (about 1.1 Trillion Naira) representing an average of 15% total annual budget would be required by the Nigerian police for a minimum of 4 years to be able to provide the services being rendered by the British police .

With the need for effective policing at moderate costing, this work finds a method of incorporating a simplified electronic policing into the existing system, with connectivity to a dedicated computerized system. The work involves the design of an Area electronic policing system for a typical local policing station covering a large area or community. At the local policing station (LPS), the information coming from any or multiples of the houses one touch information sender (OTS) [10],[11] from different zones made up of a several areas and streets are received [10],[12]. The local Area

Electronic Policing System consists of a receiver, and Local Area Electronic policing controller (LAEPC). The receiver circuit consists of an AM receiver and a comparator circuit [13].

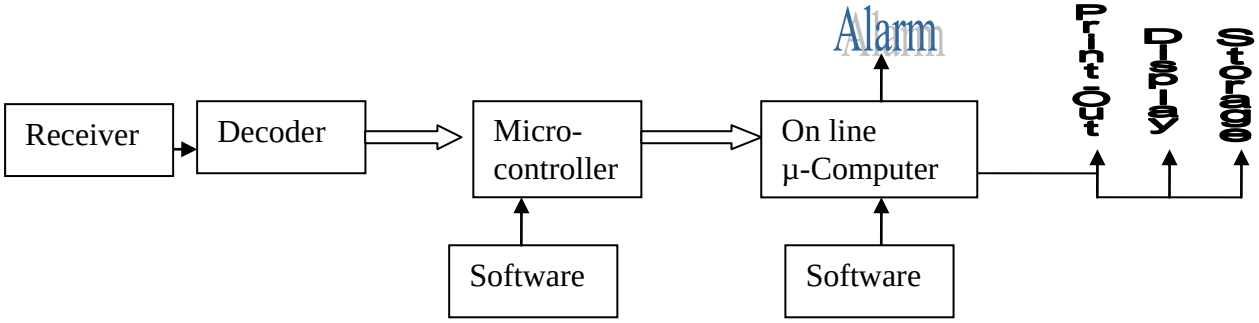

Fig 1: Simplified local area Electronic Policing System block diagram.

The basic purpose of a receiver is to receive an RF signal, amplify it, filter it to remove unwanted signals, and recover the desired base band serial information received to parallel information which is transferred to the microcontroller 80CH51 circuit [14],[15], which works on the received signals, to generate the required code, from the developed program. Since the transmitted signal from a distress point of call DPOC with the use of OTS [2] is an RF signal which through an antenna, its amplitude is very small, often in the order of a few micro-volts [12],[13].

The receiver designed is to amplify the signal from a very small level up to usable levels of several volts or more. In particular, the RF amplifier should be a low noise design because it amplifies all the low-level signals from the antenna – including noise – with a significant amount of gain. Thus the better the low-noise design of the RF amplifier, and the mixer, the better the receiver sensitivity [16]-[18].

On arrival of the information transferred by the OTS [11],[12], through the receiving antenna link at the input of the receiver and the local area LAEPC network located at the local policing station (LPS), the serial transmitted information is processed by the receiving circuit and the digital output from the op-amp comparator is transferred to the serial input of a microcontroller circuitry as shown in Fig.1. This is required to control the data base equipment which is a general purpose personal computer (PC).

The LAEPC and the PC are connected by an RS 232 interface [15] to create, through the designed software for the (PC), the output for the required information on the address, the street locations and possible outlets record needed by the policemen attached or on duty to combat the crime , in which the final success story depends on the swift response of the policemen to act on the distress call.

II. MATERIALS AND METHOD

information. The LAEPC input is the digital output signal from the receiver circuit. The LAEPC converts

A. Materials used

A Pentium III board, with 800 MHz speed, 2GB Hard disk, 128MB memory, 31/2 floppy drive, A LaserJet printer, Enhanced keyboard and mouse. An op-amp in summing mode and a FET transistor 2N4416A as the amplifier circuit with frequency tuning were used in the design with calculations made to select the circuit parameters. A diode 1N914 was used as a detector and an fsk mode of frequency modulation was developed using two separate band pass filters with an op-amp LF411CN. A comparator TLC 372D was used to generate the digital signals with digital gates, flip flops, registers and NE555 oscillator circuits used for the development of the LAEPC circuit. Multism -12 was used for the design schematics and analysis of the circuit with measurements using Oscilloscopes and Bode plotter. A Utilboard -14 software was used for the pcb development and routings.

B. Local Area Policing Receiver Circuit design

At the receiver, as the radiated electromagnetic energy passes through the antenna, a voltage is induced into the antenna that produces signal current in the input amplifiers of the receiver. The magnitude of the induced voltage depends on the intensity of the electromagnetic energy at the receiving antenna. The antenna at each end is a vital part of the wireless transmission link.

The antenna input power and power gain [16] is determined from equation 1:

$$EIRP = P_{in} A_p \qquad \ldots\ldots 1$$

For a distance of two kilometer radius from the local policing station (LPS), the power received by the receiving antenna [16],[17] is :

$$P_r = (P_t G_r G_t \lambda^2)/(16\pi^2 d^2) \qquad \ldots 2$$

where

P_r = power received

P_t = power transmitted

G_r = receiving antenna gain compared to isotropic radiator

G_t = transmitting antenna gain compared to isotropic radiator

d = distance between antennas (m)

From equation 2, the amount of power received by the antenna is [16,18]:

(If $G_r = 0.6$, $G_t = 0.6$);

$P_r = 0.36\ (P_t\lambda^2)/(16\pi^2 d^2)$

$= 0.36x\ 2.35\ (3/40\pi) = 0.36 \times 0.00134W = 0.0004824W = 0.482mW$

If the receiver has a matched impedance of 50Ω, (from $P = V^2/R$), then the voltage at the receiving end is

$V = \sqrt{PR} = \sqrt{0.02412} = 1.55 \times 10^{-1}$

$= 0.155V = 155mV$

This is a relatively strong signal because the receiver can often provide a usable output with less than 1uV signal. It is assume that , at the outer part of the coverage area , that up to 85% of the signal (in the worst case) is lost to diffraction , refraction and other signal losses [16],[17], thus , only 18mV arrives at the receiving antenna. This value was used to design the receiver system for LAEPC.

The RF amplifier designed to amplify the low level signal from the antenna is as shown in Fig. 2. At the input terminal of the amplifier, a rhombic antenna was connected which receives the signals and other surrounding signals which needed to be separated. A FET amplifier was selected to amplify the received signals from the antenna end. The choice was based on its advantages over bipolar transistors which include (i) extremely high input impedance (ii) less noise and better thermal stability [16],[18].

For a common source self biased FET amplifier as shown in Fig. 2, resistor R1 provides the leakage path to the gate current, and also serves the purpose of avoiding short circuiting of the ac-input voltage. R2 develops the gate bias. The capacitors C1 and C3 are used to couple the a.c input voltage source and the output voltage, respectively. The capacitor C2 keeps the source of the FET effectively at a.c ground and is known as by-pass capacitor [16],[17].

The a.c equivalent circuit of a common source amplifier obtained by short-circuiting the capacitors and the d.c supplies, with the FET replaced by its low frequency model [16],[17], shows that,

$$A_v = V_o / V_{in} \qquad \text{…….3}$$

And the current through R2 = R_d (by current divider rule) is

$$i_d = r_d (g_m . v_{gs}) / (R_d + r_d) \qquad \text{……4}$$

where g_m is the FET trans-conductance in mA/V or mS; and v_{gs} is the gate –to- source voltage.

The output voltage is,

$V_o = - i_d . R_d = - R_d . r_d (g_m . v_{gs}) / (R_d + r_d)$

$= - g_m . R_d \,\backslash\backslash\, r_d . v_{gs} = - g_m . r_L . v_{gs}$ …5

($r_L = (R_d \,\backslash\backslash\, r_d)$)

Thus, the output voltage,

$$V_o = - g_m . r_L . v_{in} \qquad \text{……6}$$

And the voltage gain,

$$A_v = V_o / V_{in} = - g_m . r_L \qquad \text{….7}$$

And the input resistance

$$R_i = V_{in} / i_{in} \qquad \text{….8}$$

with the output resistance

$$R'_o = (r_L = R_d \,\backslash\backslash\, r_d) \qquad \text{….9}$$

substituting the values of the parameters for 2N4416 FET : Vgs = -6v, Pd = 300mW, Vdg= 35, Vdss= 30V , Idss= 5mA and, Igss= 100pA and r_d = 100k then ;

$$r_L = R_d \,\backslash\backslash\, r_d = \frac{R_d \times r_d}{R_d + r_d}$$

$$= \frac{10 \times 100}{10 + 100}$$

$= 1000/110 = 9.09k$

From shockey's equation [17,19],

$$I_D = I_{Dss}(1 - V_{gs}/V_p)^2 \qquad \text{…. 10}$$

where ,

$$\frac{dI_D}{dI_{Dss}} = g_m = -2\, I_{Dss} \frac{(1 - V_{gs}/V_p)}{V_p} \qquad \text{… 11}$$

substituting the values of the parameters for 2N4416 FET , we have from equation 10,

$I_D = 5x\ 10^{-3}\ (1 - (-6)/(-3))^2$

$= 5mA$

Thus ,

$Rs = V_{gs}/I_p = 6/0.005 = 1.2k\Omega$

And from

$V_{Ds} = V_{DD} - I_D (R_D + R_s)$ with $V_{Ds} = V_{DD}/2$, we have

$= 9 + 6 - 5 \times 10^{-3} R_D$

and

$R_D = 2.1\ k\Omega$, in which we select 2.2 kΩ.

From equation 11,

$$g_m = \frac{-2 \times 5x\ 10^{-3}\ (1 - (-6)/(-3))}{-3}$$

$= 3.333 \times 10^{-3}\ S = 3.33mS$.

A tuned circuit amplifier offers a way to achieve gain and a particular response at high frequencies. The amplifier circuit pass-band can be controlled by the design of a resonant circuit as long as the transistor has the necessary gain. The tuned circuit for the FET amplifier was designed using equations 3 and 6, which gives a narrow band filter that passes frequencies in the range of 475- 495kHz, noting that the transmitted frequency for the design lies between 480kHz and 490kHz.

With the use of the tuned circuit design of Fig. 2 and the demodulator circuit of Fig. 3, the receiver circuit for the medium frequency was developed, which consist of the oscillator circuit, FET amplifier circuit with a tuned circuit, operational amplifiers amplifier circuits, and a comparator as shown in Fig. 4. The output from the detector, which is the frequency shift keying FSK signal generated at

the transmitting end, is fed into two separate band – pass filters; one for mark at 20kHz and the other for space at 10kHz. To extract the 10 kHz space frequency from the base-band information received after the amplification of the detected signals [8],[12],[13],[14] a band-pass filter network was designed to pass a frequency of 10 kHz. To determine the parameters of the parallel resonant band-pass circuit and the quality factor, we use equation 1, 2 and 3 to arrive at Q = f_R/ BW = 100 for a bandwidth of 100Hz . If L is taken as 10uH, we get by calculation, C = 25.36uF with Rp = 63 **Ω.**

To extract the 20kHz mark frequency, a band-pass filter network was designed with the same equations as applied to the extract of 10kHz information , but here, using a bandwidth of 200Hz, to get Q = 100, Rp =126Ω and C = 25.36uF. The output from the parallel filters are fed to a comparator circuit. A comparator is a circuit which compares an input signal Vi(t) with reference voltage Vr . When the input exceeds Vr, the comparator output voltage (Vo) takes on a value which is very different from the magnitude when Vi is smaller than Vr. If the input to an op-amp comparator is a sine wave, the output is a square wave. If a zero crossing detector is used, (i.e. when Vr is set to zero), a symmetrical waveform results [18],[19]. The output from the comparators is the digital equivalent of the coded signals sent by the transmitter circuit, and this can be transferred to a microcontroller circuit, to act as a coded signal representing an information from the transmitting end.

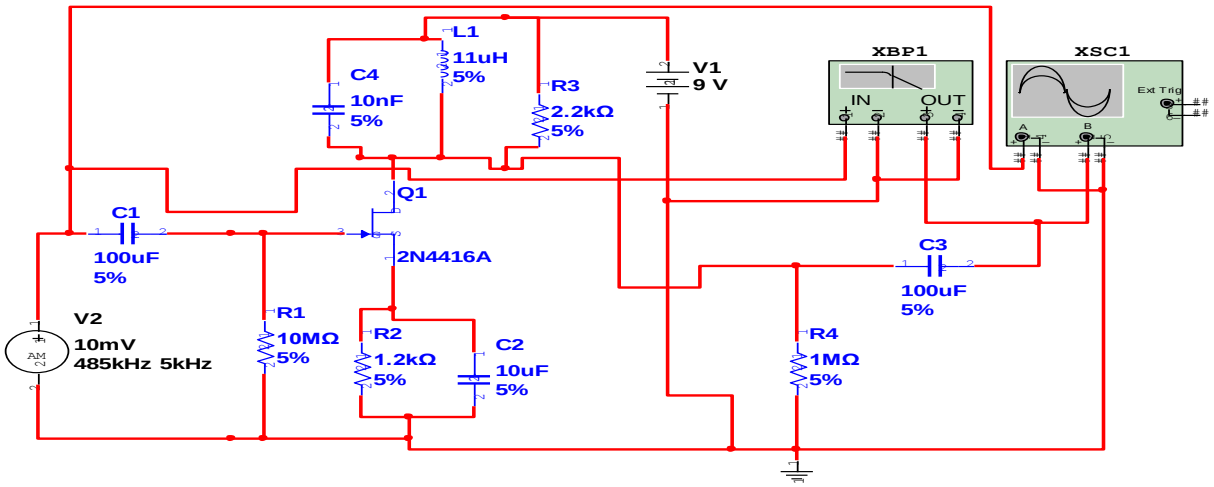

Fig 2: Tuned Circuit Receiving Circuit Design.

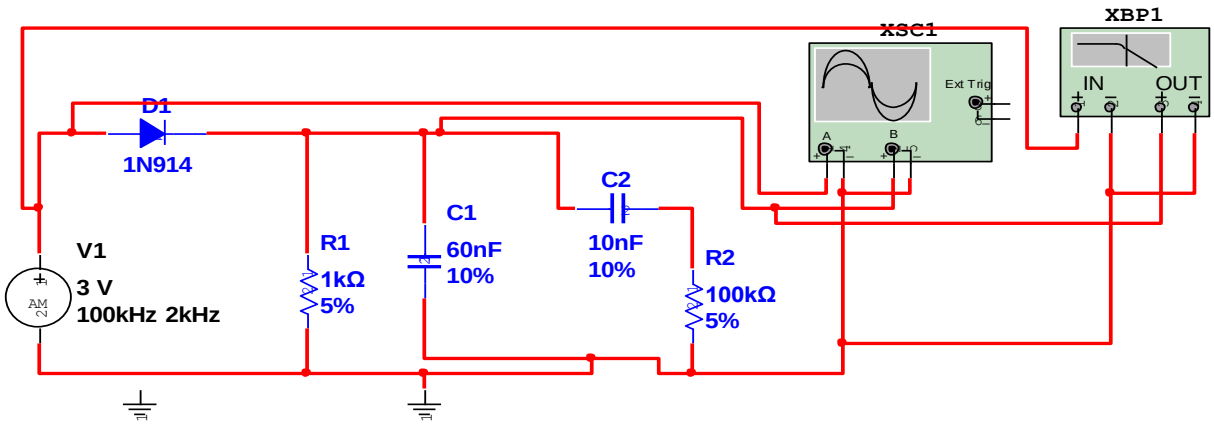

Fig 3: Diode detector circuit diagram. [7],[9]

The output from the parallel filters are fed to a comparator circuit. A comparator is a circuit which compares an input signal Vi(t) with reference voltage Vr . When the input exceeds Vr , the comparator output voltage Vo takes on a value which is very different from the magnitude when Vi is smaller than Vr.

If the input to an op-amp comparator is a sine wave, the output is a square wave. If a zero crossing detector is used, (i.e. when Vr is set to zero), a symmetrical waveform results.

The output from the comparators is the digital coded signals [20],[21] sent by the OTS, and this is transferred to the LAEPC circuit .

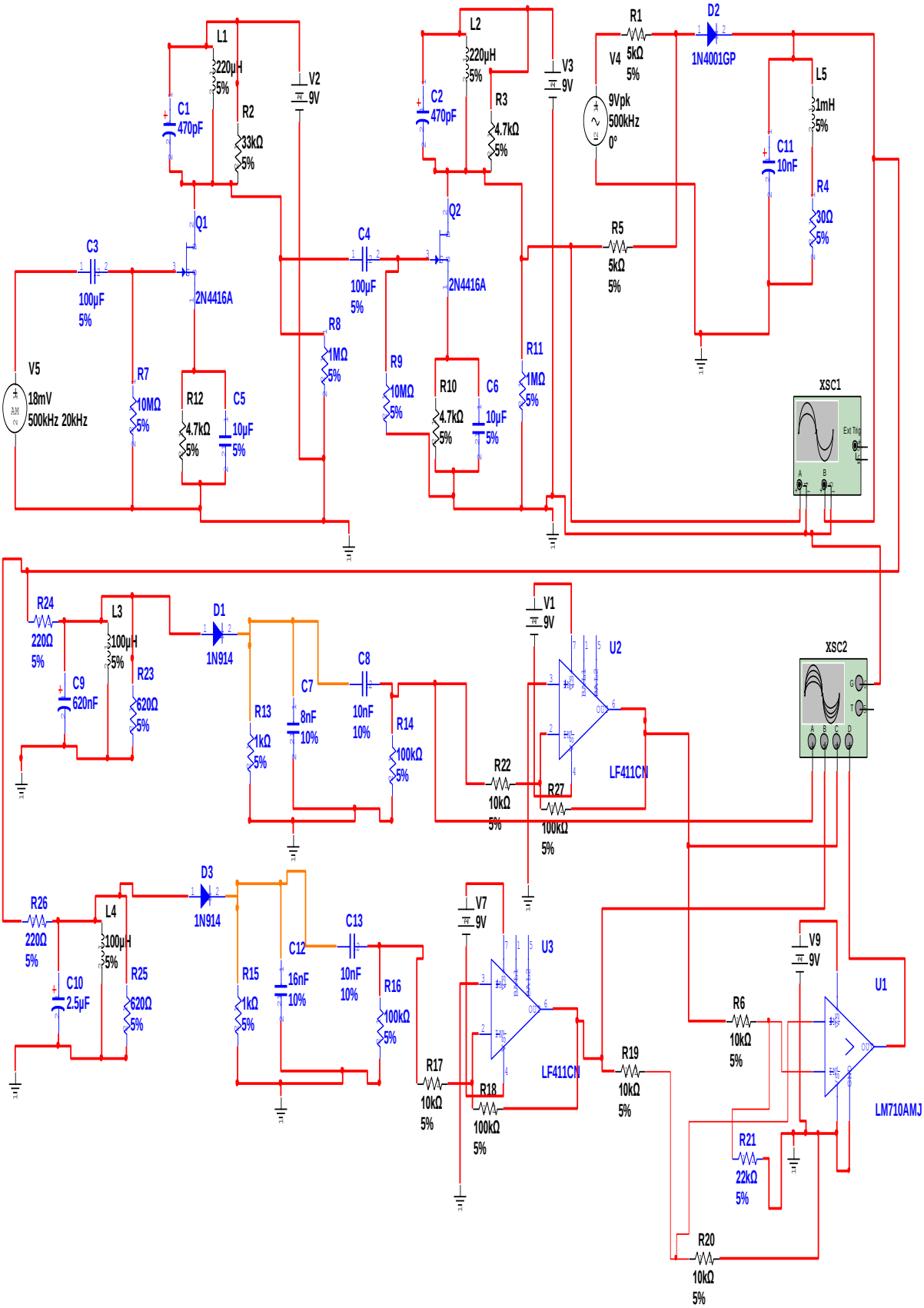

Fig 4: Receiver Circuit for the LAEPC .

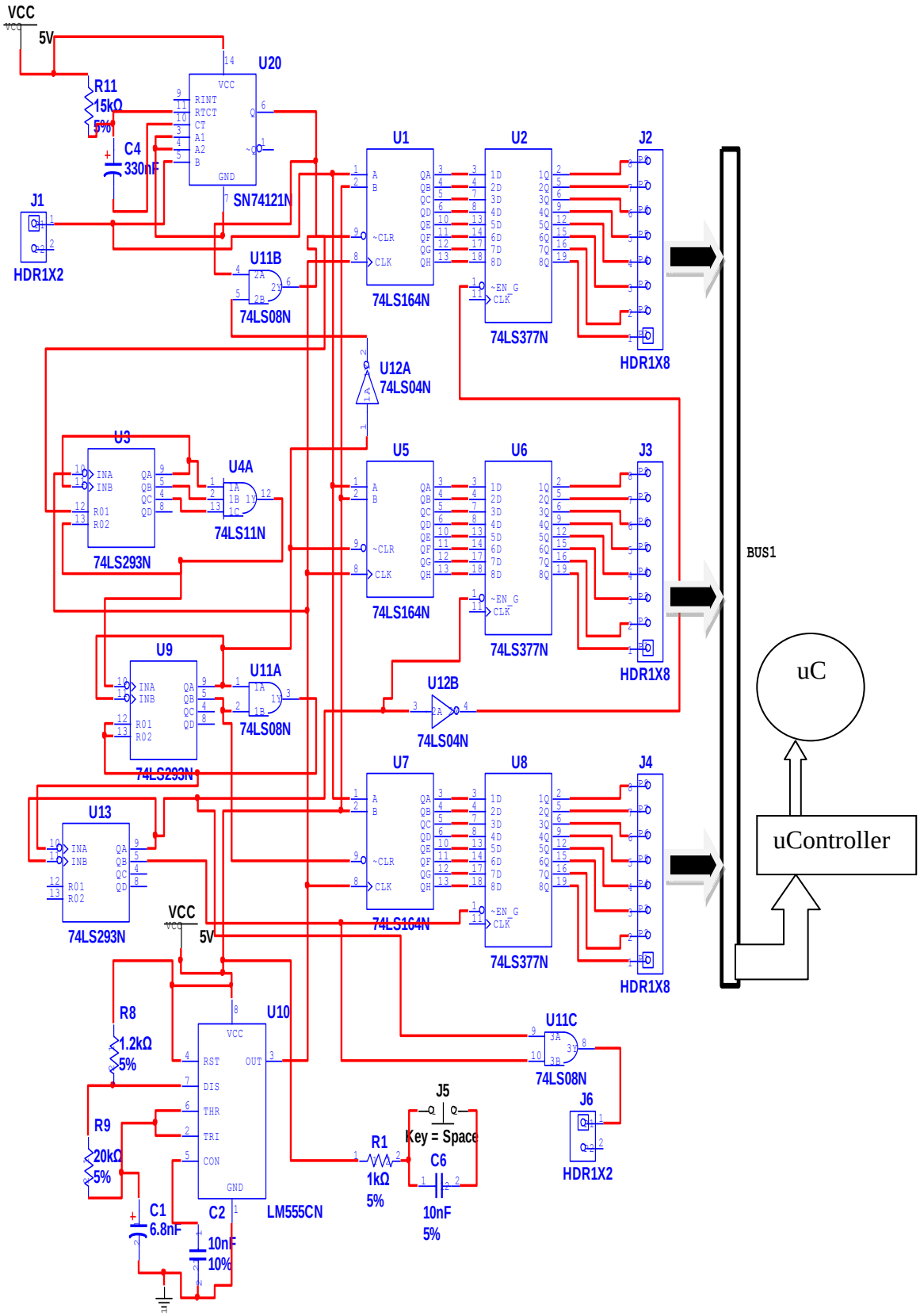

Fig 5: Circuit of a Local Area Electronic Policing Controller LAEPC

C. Local Area Electronic Policing System detailed Circuitry and operation

The information from the output of the comparators of the receiver circuit forms the input to the LAEPC. The signals which has been amplified, demodulated and filtered, forms an input to an 8 bit serial in- parallel out high speed Shift register 74LS164N U1, in which the serial data is entered through a 2-input AND gate synchronous with the LOW to HIGH transition of the clock. The control of U1 is made possible by the 4 bit asynchronous binary/decade counter 74LS293N U5, with its clock input being generated by an oscillator [20],[22] whose frequency is as same as the oscillating frequency of the one touch sender.

On the LAEPC circuit designed as shown in Fig. 5, the output of the receiver circuit is connected to a connector HDR1 X 2 (J1), which is connected to the B input of the mono-stable multi-vibrator/One shot with Schmitt trigger inputs 74LS121N (U20). The inputs A1 and A2 of the U20 is connected to ground, while the R_tC_t pin 11 of U20 is connected to a resistor R1 of 5KΩ and the C_t input connected to the anode pin of capacitor C4 of 330nf. This gives an output at pin 6, which is used as a clear input CLR of the LS164N (U1). It is to be noted that the input of J1 is also connected to pin A of U1, U5 and U7[23],[24]. The output pin 6 of U20 (121N) is connected to the A input of U11B(LS08) whose output is connected to the clear input of U1(LS164). The 2nd input of AND gate U11B(LS08) is connected to the output of the U12A inverter, whose input is connected to the CLR output of LS164N (U5) as well as the output Q_A of LS293N (U9).

The input Ro1 of U3 (LS293) is connected from the output 6 of U20 (LS121), while the Ro2 input is from the output of U4A (LS11) in which inputs to its 3-input gates is derived from Q_A,Q_B and Q_C of U3 (LS293).

The input INA of U9 (LS293N) is connected to U4A (LS11N), and INB connected to one of the inputs of a 2-input AND gate U11A (LS08N) as well as the output Q_A of U9, whose 2nd input pin is connected to Q_B output of U9 (LS293N). The output U11A (LS08N) gate is connected to INA output of U13 (LS293), with the INB of U13 connected to Q_A of U13 and EN of U6 (LS377N). The output Q_A of U13 is also used to connect U12B inverter gate whose output connects the enable input EN of the positive edge triggered D flip-flop, 8 bit TTL 74LS377N U2. The output Q_B of U13 (LS293N) is connected to the EN pin of U8 (LS377N) as well as one of the input pins of U11C(LS08N) [23],[24].

The Oscillator is an NE555 which is used to generate a 5KHZ square wave frequency with the use of resistors R_8, R_9, and capacitor C1. The output of the LM555CN oscillator pin 3 is connected to clock the CLK input of LS 164N (U1, U5 and U7) as well as INA input of 74LS293N (U3). The CLR inputs if U1, U5 and U7 are connected to U11B output, Q_A output of U9 and Q_B output of U9 respectively. The output of J2, J3 and J4 are placed on the bus (BUS 1) which forms the input of the microcontroller.

The three ICs U1, U5 and U7 74LS164 , are used to decode the 24 bits sent by the OTS to the transmission line through the transmitting medium, and its control uses the LS04N U12A and the AND gate U11B 74LS08N, which allows the first 74LS164 U1 to decode the first 8 least significant bit (LSB), and the second 74LS164 U5 decode the second 8 LSB, while the third 74LS164 U7 decode the last 8 most significant bit (MSB). The output of the three LS164 is transferred to a D-latch 74LS173 parallel-in parallel-out register with its clocks synchronized. With the clock of 74LS173 in synchronism, the output of the content of the 74LS173 is allowed to be placed on the data bus through the multiplexer of U8. The circuit diagram for the LAEPC is as shown in Fig. 7. The output from the multiplexer U8 forms an input to the 8051 microcontroller . Depending on the number of zones connected to the LPS, this zones OSR connects to a junction box J2 HDRX8 for 8 zones being covered by one LPS in this work [12]. The oscillator is an NE555 timer, which is used to generate a square wave frequency of 5kHz.

The microcontroller program for the implementation of the design is as below. The program was designed to accept two 24-bit signal to the microcontroller memory and compare the two. If the compared signals is the same, it is required of the microcomputer to transfer the signal to the networked microcomputer, and if not to raise an alarm.

D. ALGORITHM for microcontroller programming

1 Algorithm 1

1. Start (prompt for SECURITY 1 Data - 24 bits)
2. Receive the first 8 bits and store in memory location SECURITY 1 (LSB)
3. Receive the second 8 bits and store in memory location SECURITY 1
4. Receive the third 8 bits and store in memory location SECURITY 1 (MSB)
5. (Prompt for SECURITY 2 Data - 24 bits)
6. Receive the first 8 bits and store in memory location SECURITY 2 (LSB)
7. Receive the second 8 bits and store in memory location SECURITY 2
8. Receive the third 8 bits and store in memory location SECURITY 2 (MSB)

2 OPERATION Methodology For The Microcontroller

1. Compare SECURITY 1 Data with SECURITY 2 Data
2. If the same, move SECURITY Data 1 to output port in this order

a. The first 8 bits of SECURITY Data 1 to equate Data A
b. The second 8 bits to Accumulator
c. The first 4 bits of the data in Accumulator to equate to Data B
d. The second 4 bits of the data in Accumulator to equate to data C
e. Move Data B and Data C to output 1 port
f. Clear the Accumulator
g. The 8 bits to Accumulator
h. The first 4 bits of the data in Accumulator to equate to data D
i. The second 4 bits of the data in Accumulator to equate to data E
j. Move Data D and Data to E to output 1 port

3. Go to Start
4. Else

a. Move or load Accumulator with 0/h
b. Output 2 0/h to trigger alarm

End

3 Algorithm 2

1. Initialization

* Set port as input and the other port as output
* Ensure Synchronization of data through the serial transmission

PORT 3 EQU input port 1, PORT 2 EQU output port 2 for Alarm

2. START

a. Declare your data

SECURITY 1 Data equ 3 bytes
SECURITY 2 Data equ 3 bytes
Data A equ first byte of SECURITY 1 Data
Data B equ first 4 bits of 2nd byte of SECURITY 1 Data
Data C equ second 4 bits of 2nd byte of SECURITY 1 Data
Data D equ first 4 bits of 3rd byte of SECURITY 1 Data
Data E equ second 4 bits of 3rd byte of SECURITY 1 Data
ALARM equ 0/h

b. Prompt for SECURITY DATA from the interface device.
c. Receive SECURITY 1 Data in sequence and store in a memory location
d. Receive SECURITY 2 Data in sequence and store in a memory location

4 Operation Methodology For The Output

a. Compare SECURITY 1 Data with SECURITY 2 Data
b. If the same,

* Output Data A to E in sequence
* Start again

c. Else

* Output ALARM
* Wait for RESET
* Start again

5 Algorithm 3

Operations

1. Micro-controller to wait for an interrupt the device that will send data as its readiness to transmit data to the microcontroller.
2. Micro-controller acknowledges interrupt by enabling itself to receive the data
3. After receiving all the data, it closes the reception for further processing
4. Compare the data received; if the same continue 5, else trigger alarm
5. Wait and send a request to send signal to the computer
6. Acknowledge the RTS from the Computer
7. Send the data in sequence and acknowledge its reception by the PC
8. After sending all data, the u-controller restarts at 1

3.6.4 Operations Program for the microcontroller

Module

1. u-controller to wait for an interrupt from the device that will send data

Module

2. Acknowledges interrupt and initiate the process of receiving data

Module 3

3. Receive all data and store the data received

Module

4. Compares the data received; if the same continue and segment the data
received into A to E, else trigger alarm

Module

5. Send RTS signal to PC

Module

6. Acknowledge the RTS signal from PC

Module

7. Send the data in sequence and acknowledge the reception of each segment by the PC

Module

8. After sending all data, the micro-controller restarts at step 1

6 *Programming the microcontroller*

Head : This program is designed to accept 2-24 bit data, compare this data, if the same, transfer the 24 bit data to a PC and if not the same, trigger an alarm.

For error detection and correction, redundancy error of transmitting twice [21] was used, in which case, the coded information is transmitted 2 times, and the microcontroller compares the 2 information received, if same, to allow for further processing and , if , otherwise a signal is generated to ring an alarm. It is believed in this work according to statistics and response from interviews, that, the probability of 2 or 3 consecutive robbery operation going on at the same local area being policed is very low if not zero. This is because, all the reported cases in the same environment [12], shows that same robbery gang do operate in sequence in one environment at a given time.

III. RELIABILITY TESTING

One indicator to test the reliability of equipment is the rate at which the equipment fails which is called the failure rate. Failure rate is normally defined by the mathematical relation,

$\Lambda(t) = \lim 1/Ns \times \Delta Nf/\Delta t = 1/Ns \times dNf/dt$ ……11

where, Ns = number of surviving components after a life test

ΔNf =number of failed components during the time interval, Δt.

Component failure rates are normally affected by the mechanical, electrical , and thermal environments in which they are required to operate [26],[27]. Shock and vibration have relative small effect on the electronic components with small size. For this reason, the effect of environment, temperature , and operational stress on the failure rate of each component in an equipment is accounted for by introducing multiplying coefficients W_E ,W_T , W_R known as weighing factors due to environment, temperature and rating [26],[27].

When an equipment operates under an unfavourable condition , the relevant weighing factor is greater than unity (> 1); whereas for an equipment operating under favourable condition the weighing factor is less than or equal to unity[26],[28].

The overall failure rate of each component, λ_0 in an equipment can be obtained as

$\lambda_0 = \lambda\, n\, W_E\, W_T\, W_R$ ……12

where

λ = basic failure rate

n = quantity of the same component in the equipment

W_E = weighing factor due to environment (other than temperature)

W_T = weighing factor due to temperature

W_R = weighing factor due to rating

Numerical values are usually given as the W_E ,W_T , W_R for computational purpose [26].

Thus, the overall total failure rate of an equipment can be obtained by adding up the overall failure rates contributed by all the individual components in the equipment, i.e.

$\Lambda_T = \lambda_{01} + \lambda_{02} + \lambda_{03} + \ldots\ldots,+ \lambda_{0n}$ ….13

If failure rate is constant, the probability of no failures occurring in a given time t is

$R = e^{-\lambda t}$ …14

Where R(Reliability) is the probability of no failures occurring in a given time t .

This reliability assessment was used to determine the reliability of the designed LAEPC .

IV. RESULTS

A. *The local area policing controller*

The response of the receiving RF amplifier is as shown in Fig. 6 giving an output voltage of 660mV, which is further amplified using the common source FET amplifier , to give an output of about 4.5V, as shown in Fig. 7. The bode-plot response of the receiver to the incoming signals using a FET tuned circuit is as shown in Fig. 8. The peak voltage measured is 4.5V. This voltage is enough to drive the AM diode detector whose forward voltage response is 0.7V. The bode-plot response of the receiver to the incoming signals using a FET tuned circuit in Figure 8 shows that only frequencies above 470kHz and below 495kHz are allowed to pass through the network with a resonant frequency of 483.553 kHz and a gain of 27.734dB, while others are totally attenuated. The output voltage from the diode detector circuit is 1.32V, as measured by the oscilloscope, and this voltage is amplified using the FET rf amplifier circuit. The output from the detector is the frequency shift keying signal transmitted from the OTS at a voltage of 8.5V and 7.4V. The output of the two separated parallel filters was fed into a comparator circuit which gives a response shown in Fig. 9. When the 20kHz representing the mark frequency (or the High State of the transmitted information) passes through the circuit, a voltage of 5V is achieved and when the frequency is changed to 10kHz, the voltage is in its reference voltage level of OV.

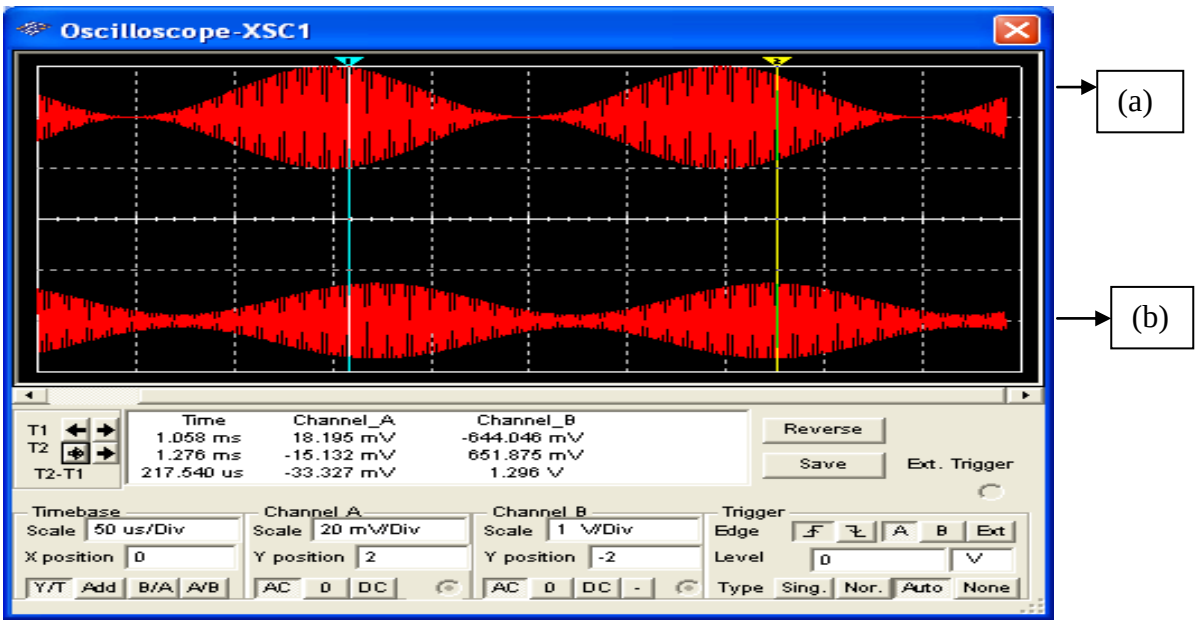

Fig 6: Waveform Of The FET Receiving Amplifier Response

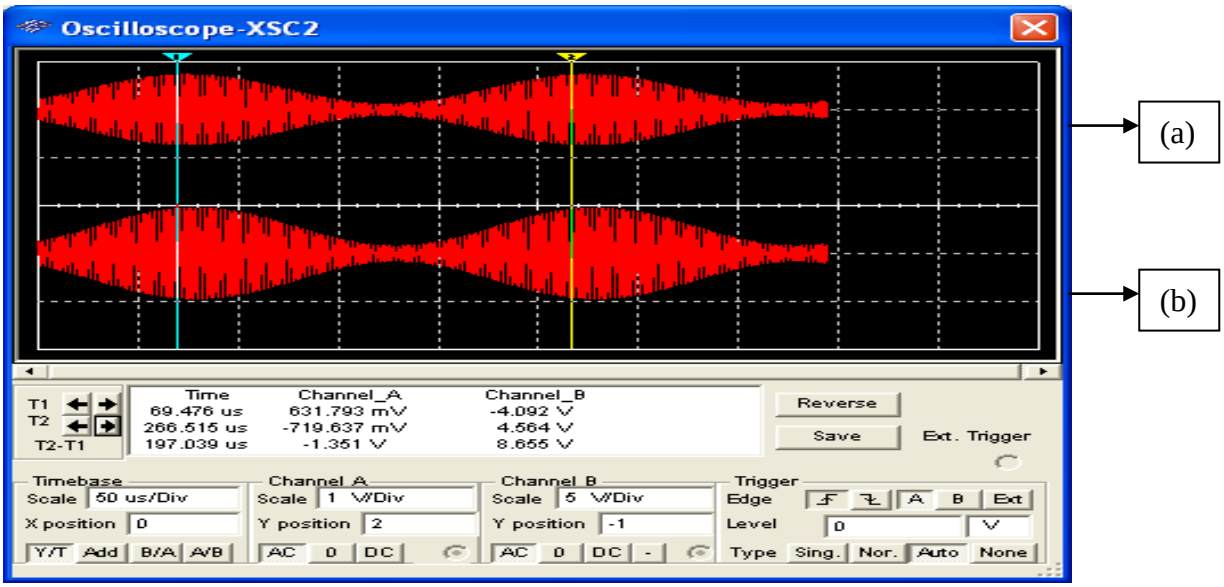

Fig 7: Amplification Of RF Amplifiers Output Voltage To 4.5V Using FET Amplifier.

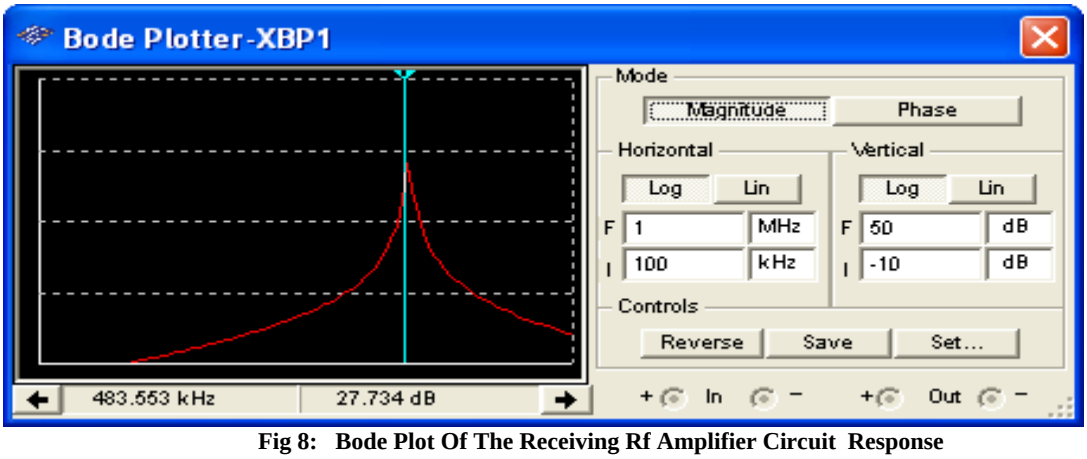

Fig 8: Bode Plot Of The Receiving Rf Amplifier Circuit Response

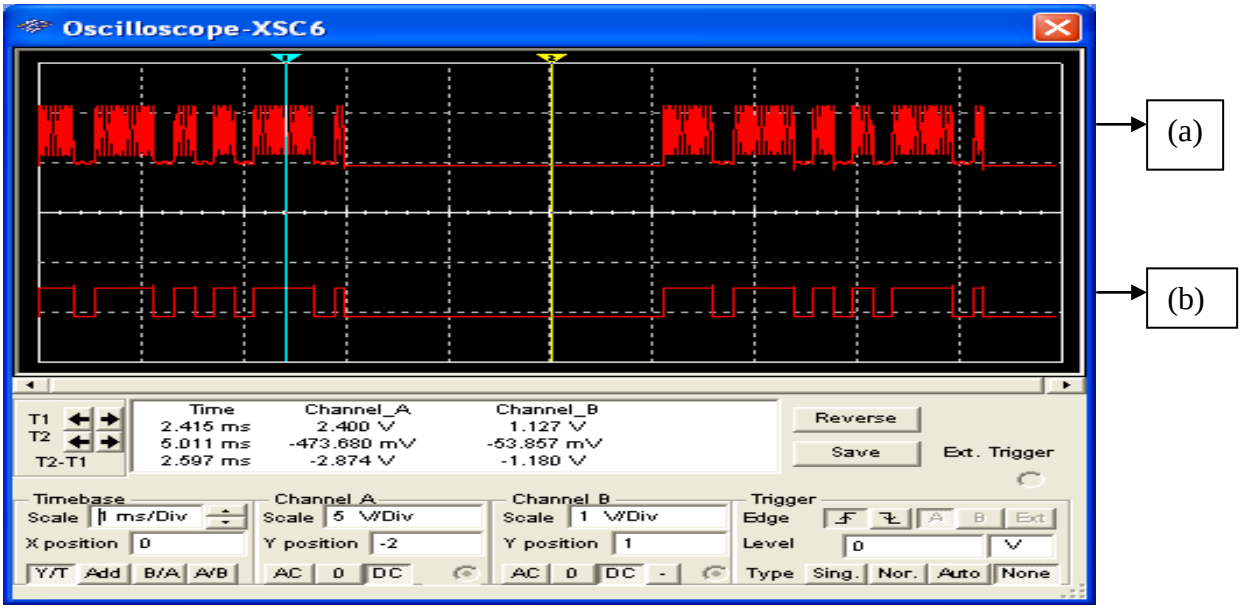

Fig 9: a). output from the 20kHz filter, b). The comparators output giving the digital signals.

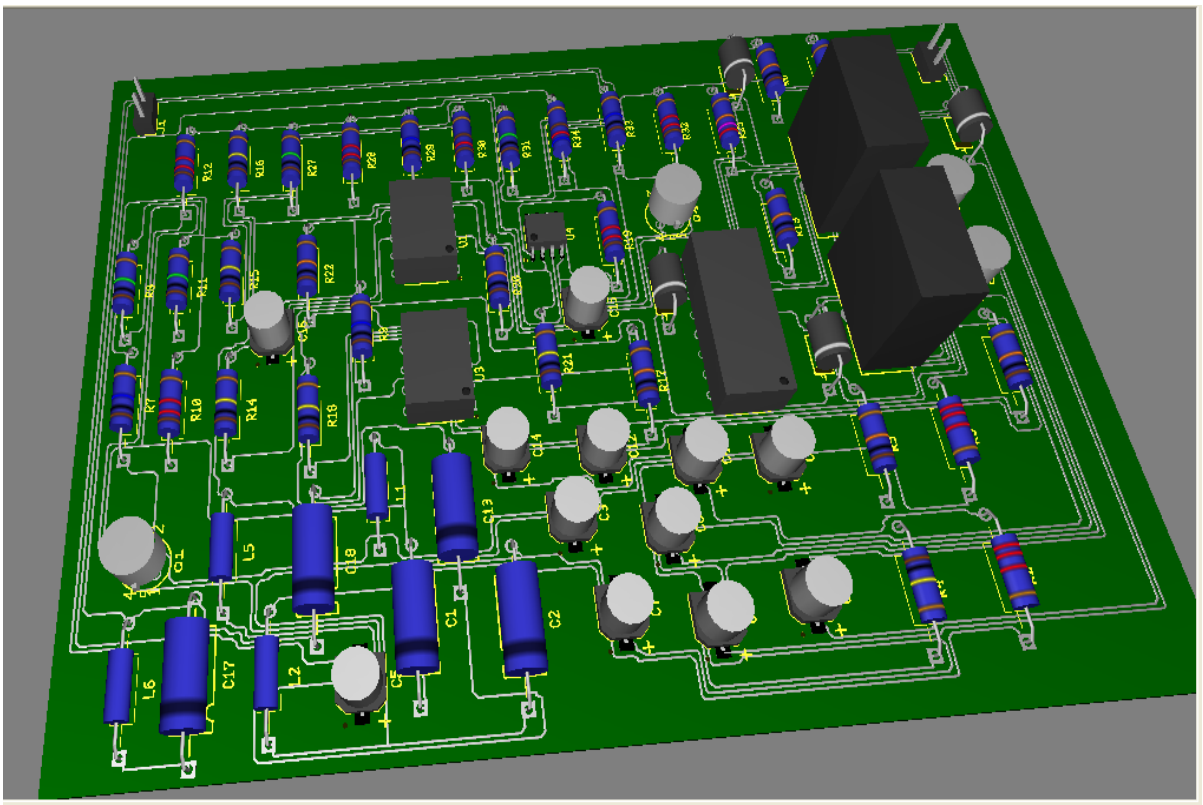

Fig 10: Simulated LAEPC receiver PCB design layout and placement [29].

Table 1. Schematic statistics report on LAEPC receiver pcb placement

Schematic Statistics Report (From Document: receiver for laepc

	Name	Quantity
1	Number of components	88
2	Number of real components	70
3	Number of virtual components	18
4	Number of gates	2
5	Number of nets	46
6	Number of pins in nets	184
7	Number of unconnected pins	5
8	Total number of pins	189
9	Number of pages	1
10	Number of HB instances	0
11	Number of unique HBs	0
12	Number of SB instances	0
13	Number of unique SBs	0

Table 2. List of Components used for LAEPC circuits and reference designation.

	Quantity	Description	RefDes
1	3	74LS, 74LS164N	U1, U5, U7
2	3	74LS, 74LS377N	U2, U6, U8
3	3	74LS, 74LS293N	U3, U9, U13
4	1	74LS, 74LS11N	U4
5	2	CONNECTORS, HDR1X2	J1, J6
6	3	CONNECTORS, HDR1X8	J2, J3, J4
7	1	TIMER, LM555CN	U10
8	1	RESISTOR, 20kΩ 5%	R9
9	1	CAPACITOR, 10nF 10%	C2
10	1	RESISTOR, 1.2kΩ 5%	R8
11	1	CAP_ELECTROLIT, 6.8nF	C1
12	1	MULTIVIBRATORS, SN74121N	U20
13	1	RESISTOR, 15kΩ 5%	R11
14	1	CAP_ELECTROLIT, 330nF	C4
15	1	CAPACITOR, 10nF 5%	C6
16	1	RESISTOR, 1kΩ 5%	R1
17	1	74LS, 74LS08N	U11
18	1	74LS, 74LS04N	U12

Table 3. Schematic statistics report on LAEPC circuit pcb placement.

	Name	Quantity
1	Components	31
2	Real components	27
3	Virtual components	4
4	Gates	6
5	Nets	75
6	Pins in nets	214
7	Unconnected pins	14
8	Total pins	228
9	Pages	1
10	Hierarchical block instances	0
11	Unique hierarchical blocks	0
12	Subcircuit instances	0
13	Unique subcircuits	0
14	Unique hierarchical blocks in PLDs	0
15	PLD hierarchical block instances	0
16	Unique subcircuits in PLDs	0
17	PLD subcircuit instances	0

This digital signal of Fig. 9b forms an input signal to the LAEPC circuit which is in serial form. The serial digital information from the receiver, being fed into the local Area policing Controller input is processed and the parallel output is transmitted to the data bus , which is transferred to the microcontroller , with the software developed, with the use of the program written, and the output coded signal transferred to the on –line microcomputer for interpretation. The simulated LAEPC receiver PCB layout and placement design is as shown in Fig. 10, in which the statistical report of the pcb layout is as shown in Table 1. The simulated LAEPC circuit PCB layout and placement design is as shown in Fig. 11, in which the statistical report of the pcb layout is as shown in Table 3.

With the use of redundancy error detection method, the software detects whether or not there is an error in the received signal.

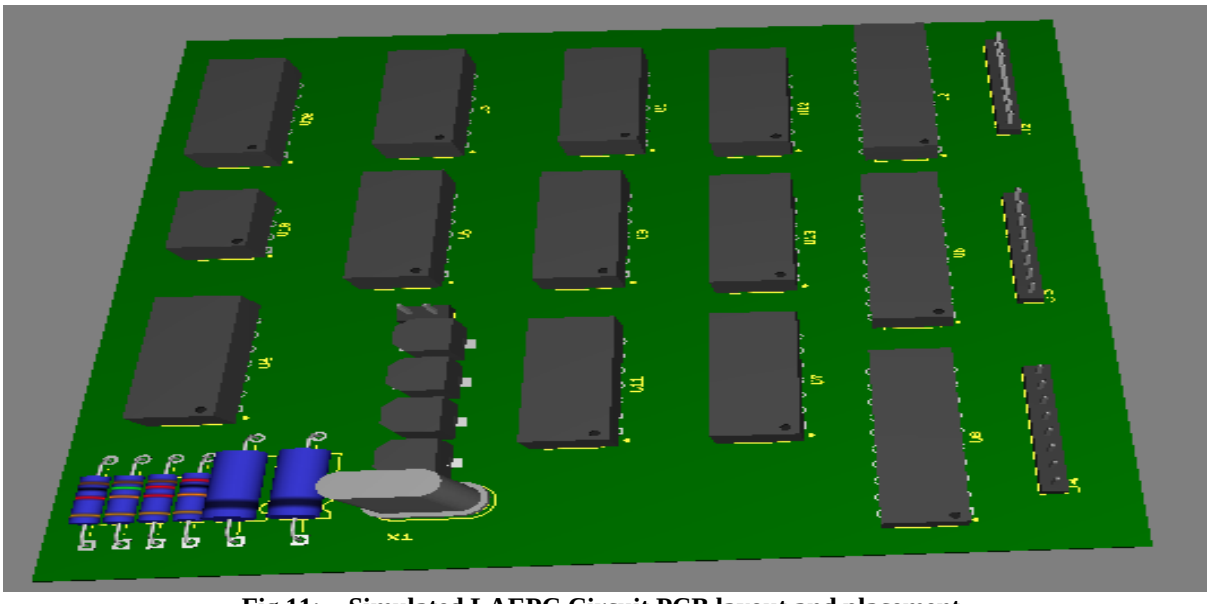

Fig 11: Simulated LAEPC Circuit PCB layout and placement

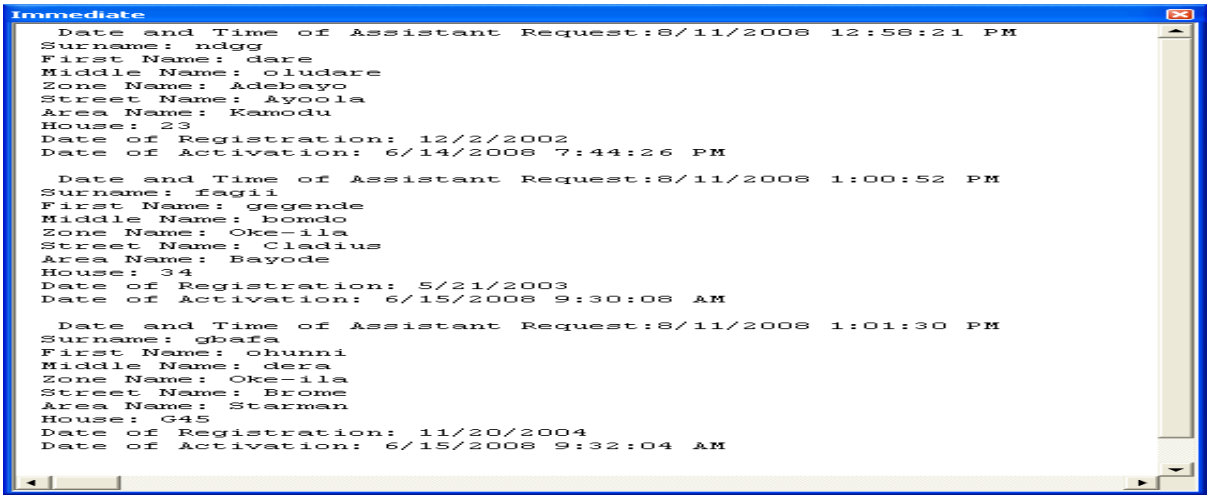

Fig 12: Records of request with details as recorded in the LPS computer database.

Table 4. Failure rate of LAEPC receiver circuit determination.

Components	Number used	Basic Failure Rate, λ (% /10^3 hr)	Weighing factors due to Enviro. W_e	Temp W_t	Rating W_r	Overall failure rate, (% /10^3 hr) $\lambda oi = n_i \lambda i W_e W_t W_r$
Transistors	04	0.008	2.0	1.5	2.0	0.192
Diodes	04	0.005	2.0	1.5	1.5	0.090
Capacitors	17	0.01	2.0	1.5	3.0	1.53
Resistors	33	0.005	2.0	1.5	2.0	0.99
Connectors	184	0.001	2.0	1.5	-	0.552
Switches micro		0.001	-	-	-	-
IC's	03	0.002	-	-	-	0.006

The transferred code from the microcontroller to an on-line micro-computer is being used to locate the DPOC address and the records of request with details as recorded in the system database as shown in Fig. 12.

B. Reliability assessment of designed LAEPC

For the local area policing controller LAEPC receiver circuit , the reliability of the system is determined for a 1 year continuous operating period was calculated with weighing factors and ratings with the use of Table 4 [27],[28].

From, equation 12,
$\lambda_T = \sum \lambda oi = 3.36\ \% /10^3\ hr = 0.0336 /10^3\ hr$

from these result, we obtain the system overall failure rate as $\lambda_T = 3.336\ \% /10^3$ hr
or $\lambda_T = 0.0336 /10^3$ hr

For an average operating time of 1 year, t = 1 x 365.4 x 24 = 8760 hrs

Thus , the reliability of this system from equation 14 is,

$R = e^{-\lambda t} = e^{-(0.0336 \times 0.001 \times 8760)} = e^{-(0.294)}$
$= 0.745 = 74.5\ \%$.

For the reliability of the LAEPC circuit, with the use of equation 12, 13 and 14;
R = 0.934 = 93..4%
While the combine reliability of the receiver and LAEPC circuit is calculated as ,
R = 82.6%.

The reliability result is for a worst case situation, in which the receiver and LAEPC is under continuous operation through-out the year round. It must be noted that C and R used in the system design contributes over 71% of the overall failure rate in both. Thus, if these are well rated, the reliability increases considerably. Also, if the connectors are well routed on the PCB to reduce damage, the reliability of the system can increase to 96.5%. This compares favourably with the Chinese product designs whose reliability assessment ranges between 50 and 70% for cost benefits [26].

V. CONCLUSION

A local Electronic policing System was designed consisting of the receiver circuit to receive information from any or multiple houses within the network coverage using a one touch sender [10] from different zones and streets , and a local area electronic

policing controller to convert the serial information received from the receiver circuit to a parallel information which is transferred to the microcontroller circuit to generate the required code from the developed program. The microcontroller program for the implementation of the design was developed to accept two 24-bit signal to the microcontroller memory and compare the two, and if the compared signals is the same, it is required of the microcomputer to transfer the signal to the networked microcomputer, and if not to raise an alarm.

The transferred code from the microcontroller to an on-line micro-computer is being used to locate the DPOC address and relevant information from the system database.

The designed LAEPC with its attachments in conjunction with the use of OTS, will increase the "caught- in the –act" scheme as against the present "after –the- act " investigations being adopted by the Police to combat crime in developing countries. The "caught- in the –act" scheme is necessary to prove the case of criminality beyond any reasonable doubt, in a law court.

For the local area policing system consisting of a receiver and LAEPC , the reliability of the system was determined for a 1 year continuous operating period with weighing factors and ratings to give 82.6%.

With the use of utilboard -10, a professional electronic design routing and manufacturing software, the design can easily be transferred ,etched on a positive photo-resist board , and be manufactured in developing nations like Nigeria , with the result of vast employment generation to hundreds directly, and multiples indirectly.

With all the stated , it is to be noted that the success of this design in achieving the purpose meant for, depends on the immediate and "direct to spot" of incidence of distress call, by the Police, with the electronic dispatch bill of policing developed. Prompt response to details on point of call of distress is expected , and lack of response by the Police team is expected to be out- lawed by review and amendments of police act, to stipulate tougher penalty on the officers concerned, and ,with this put in place, a safer environment is envisaged.

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